Appl. No. 09/527,634 Amdt. dated February 13, 2004 Reply to Office Action of November 13, 2003

## **REMARKS/ARGUMENTS**

Claims 1-13 are pending in this application. Claims 7-10 have been allowed, and claims 3 and 4 have been indicated as allowable if rewritten in independent form. Independent claims 1 and 13 have been amended to further clarify the distinctions of the present invention over the cited art.

## Michael et al. (5,287,458).

The rejected claims have been rejected as anticipated by Michael, or obvious in view of Michael and other references. The present invention is directed to minimizing the delay time between transmission of data from a UART and the subsequent reception of data in the other direction. Michael, on the other hand, is directing to loading additional words for transmission into a UART and for minimizing the number of interrupts to a processor to indicate that more data is ready to be received by the UART. See, for example, the Background in col. 1, line 60 to col. 2, line 2 for a description of the loading of new data into the UART. See the Summary of the Invention, lines 42-54 for a reference to the desire to avoid multiple interrupts.

Claim 1 has been amended in two respects. First, the control signal in the transmitter empty circuit clause has been amended to indicate that it relates to the availability of the serial transmission line "to receive data". This is to be distinguished from loading additional words into the UART for transmission. Additionally, the delay circuit clause has been amended to clarify that the delay time is "related to transmission characteristics of said serial transmission line." In Michael, in contrast, the purpose of the delay is to eliminate multiple interrupts for a Transmitter FIFO Empty condition (see col. 15, ll. 46-49).

Also, the delay time in Michael excludes the extra Stop bit time. "The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs..." (col. 15, ll. 38-40). Thus, the variable number of Stop bits noted in the Office action in col. 5 is not used to produce the delay time referred to in col. 15.

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Because of the multiple differences between the present invention and Michael as discussed above, and the amendments to the claims, it is believed that Michael does not anticipate nor make obvious the present invention. The other cited references do not provide the features missing from Michael, and accordingly, all the claims are believed to distinguish Michael and the other cited references.

## **CONCLUSION**

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted

Paul C. Haughey

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, Eighth Floor San Francisco, California 94111-3834

Tel: 650-326-2400 Fax: 415-576-0300

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